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Design & Performance Analysis of DG-MOSFET for Reduction of Short Channel Effect over Bulk MOSFET at 20nm

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ABSTRACT
An aggressive scaling of conventional MOSFETs channel length reduces below 100nm and gate oxide thickness below 3nm to improved performance and packaging density. Due to this scaling short channel effect (SCEs) like threshold voltage, Subthreshold slope, ON current and OFF current plays a major role in determining the performance of scaled devices. The double gate (DG) MOSFETS are electro-statically superior to a single gate (SG) MOSFET and allows for additional gate length scaling. Simulation work on both devices has been carried out and presented in paper. The comparative study had been carried out for threshold voltage (V_T), Subthreshold slope (Sub V_T), I_{ON} and I_{OFF} Current. It is observed that DG MOSFET provide good control on leakage current over conventional Bulk (Single Gate) MOSFET. The V_T (Threshold Voltage) is 2.7 times greater than & I_{ON} of DG MOSFET is 2.2 times smaller than the conventional Bulk (Single Gate) MOSFET.

Keywords **-** DG MOSFET (Double Gate Metal oxide Field Effect Transistor), Short Channel Effect (SCE), Bulk (Single Gate) MOSFET.

I. INTRODUCTION

The downscaling of metal-oxide-semiconductor field-effect transistor, MOSFET has been popular for decades ago to get the well circuit performance and to suit Moore's law as well as the direction shown by International Technology Roadmap for Semiconductor, ITRS 2012. From last 4 decade, semiconductor device technology has changed with an amazing speed [1]. There is an exponential growth in integrated circuit performance, the scaling of MOSFET dimensions and its structure has been the primary driver. From the vantage point of today, in the 45 nm process era, we look 5 years into the future and find that the double-gate MOSFET (DG-MOSFET) is widely expected to take over for the long-lasting industrial favorite, than the single-gate MOSFET [2]. As scaling is expected to reach the 14 nm era in a few years, the DGMOSFET becomes necessary in terms of its superior properties in this scaling region [3].Current CMOS technology, conventional MOSFET will be difficult to scale further, even if we use high-k gate dielectrics, metal electrodes, strained silicon and other new materials being considered. Multi Gate Field Effect Transistor (MUGFET) is thought to be the leading new transistor technology which will take over as the leading workhorse in digital electronics. International Technology Roadmap for Semiconductor, devices with gate lengths down to 10 nm can be expected in 2019 [3&6].In fact, over the past 3 decades the number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced. For example 45 nm technology node will have double MOSFETs in a microprocessor than a 65 nm technology node [4].

As MOSFET geometries shrink, the voltage that can be applied to the gate must be reduced to maintain reliability. To reduce the power, the threshold voltage of the MOSFET has to be reduced, but As threshold voltage is decreased, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available. Hence sub threshold leakage current is major issue of modern high-performance VLSI chips [5].

A. Double Gate MOSFET

Single gate device at nanoscale is suffering from short channel effect that can be overcome by various multi gate structures like Double Gate, trigate & Gate All Around structure. The double gate (DG) MOSFETs are electro-statically superior to a single gate (SG) MOSFET and allows for additional gate length scaling [1]. The DG MOSFETs are the devices, which are having two gates on either side of the channel. One in upper side, known as top gate and another one is in the lower side of the channel, known as bottom gate. It gives better control of the channel by the gate electrodes [8]. This ensures that no part of the channel is far away from a gate electrode. The Double- Gate MOSFET (DGMOSFET) structure minimizes short-channel effects that allows more aggressive device downscaling of device up to 10 nm gate length [2]. There are two structures for modeling gate structure i.e Planar& Non-planar [6].

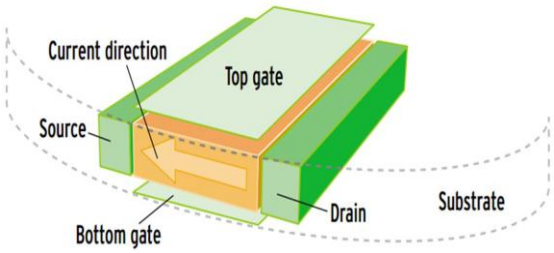


Fig. 1. Schematics of a DG MOSFET with a planar structure

The Advantages of using planar structure is better uniformity of Silicon channel thickness & can use existing fabrication processes. Disadvantages are fabrication of back gate and gate dielectric underneath the Silicon channel is difficult & accessing bottom gate for device wiring is not easy (may impact device density).Structure shown in fig.1.

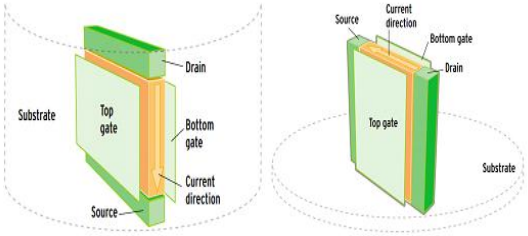
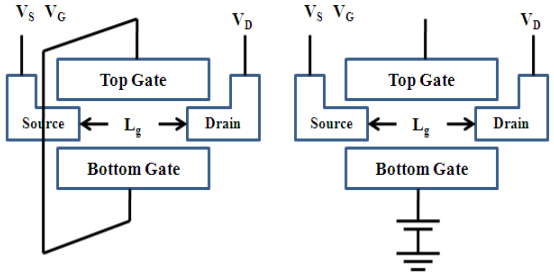


Fig. 2. Schematics of a DG MOSFET with a non-planar structure.

The advantage of using non- planar structure (Shown in fig. 2) is the easier formation and access of both gates (wraparound gate) & increases device density. Disadvantage are channel thickness defined by lithography (poorer uniformity) front and back gates cannot be independently biased& from conventional fabrication processes [6].

As planar structure is easy to design, the DG planar structure is used for design & stimulation. The voltage applied on the gate terminals controls the electric field and determining the current flowing through the channel. Fig. 3 shows that there are two mode of operation (a) to switch both gates simultaneously (b) to switch only one and apply a bias to the second gate (this is called ("ground plane" (GP) or "back-gate" (BG)) [5].



(a) (b)

Fig. 3. General Operation of DG MOSFET structure

II. DESIGN OF DOUBLE GATE MOSFET (DG-MOSFET)

For designing the proposed device and its simulation, ATLAS device simulator tool of Silvaco TCAD is used.

A. Device Design

The proposed device is Double Gate MOSFET with gate length Lg of 20nm, gate oxide thickness of 1nm, metal gate with work function explicitly set to 4.17 eV, heavily n-doped (ND=1e+21 CM-3) source and drain region, Si is the channel material with channel doped (ND=1.5e+19 CM-3) and SiO2 is the gate dielectric as per the ITRS 2012 road map. Fig.4 & Fig. 5 shows the designed DG-MOSFET in Silvaco TCAD tool.

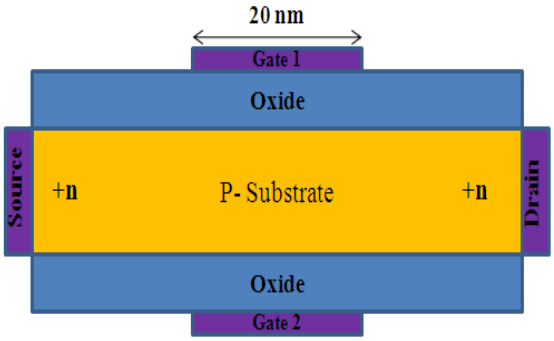


Fig. 4. Schematic structure of DG MOSFET with gate length of 20nm

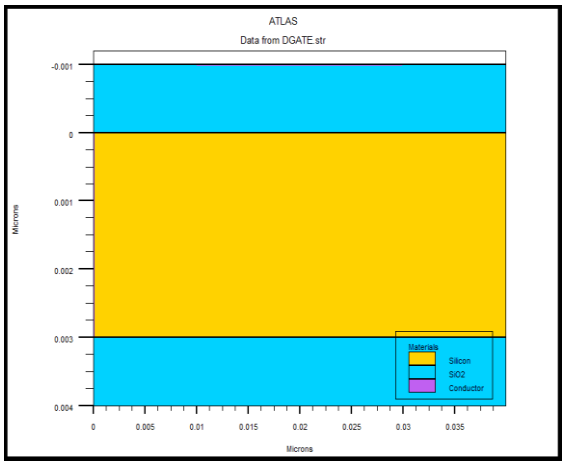


Fig. 5. Two Dimensional Device Structure of DG MOSFET

B. Device Simulation

The modeled device is simulated to obtain the output (I_{DS} versus V_{GS} curve) and (I_{DS} versus V_{DS} curve) for DG MOSFET. Furthermore, some parameters are extracted such as V_T, Sub-threshold, ON current and OFF Current.

I_{DS}- V_{GS} characteristics

The Two models as Shockley-Read-Hall (SRH) model and Lombardi model (CVT) are recommended

for physical models for MOS type FETs. For mathematical simulation calculation model, the program select model NEWTON and GUMMEL with maximum trap 4. To generate I_{DS} versus V_{GS} characteristics curve, it is done by obtaining solutions at each step bias points first and then solving over the swept bias variable at each stepped point. V_{DS} value are obtained with V_{GS} = 1.0 V. The outputs from these solutions are saved in .log file (solution file). For each drain bias, .log file is loaded and ramped the gate voltage is performed. The drain voltage (V_{DD}) is set to 0.1 V while gate voltage (V_{GS}) is ramped from0 V to 1.0 V by a voltage step of 0.1V. Finally, one I_{DS}- V_{GS} curves are overlaid using Tony Plot as shown in fig. 6. DG MOSFET. V_{DD}= 0.1 V was chosen to see the current at conduction (inversion layer exists), but at low electric field.

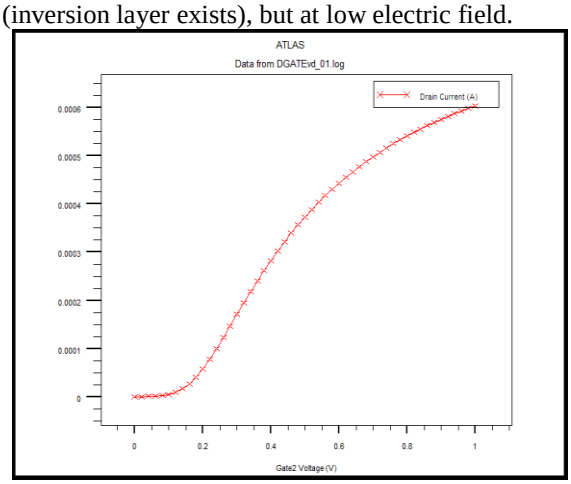


Fig. 6. Transfer characteristics for DG MOSFET with L = 20 nm for V_{DD} =0.1 V, tox= 1 nm

I_{DS}- V_{DS} characteristics

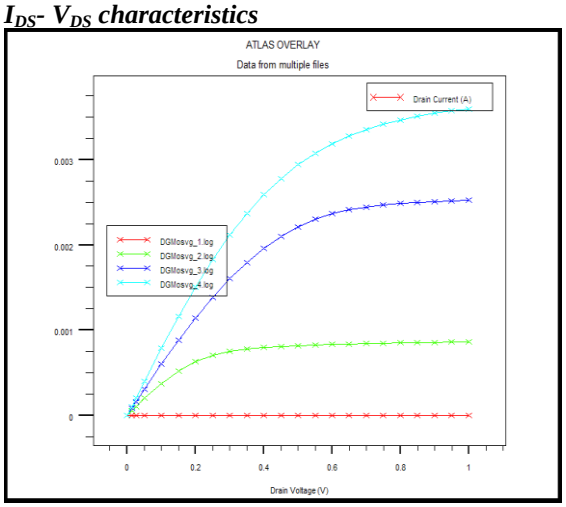


Fig. 7. I_{DS} versus V_{DS} of DG MOSFET parameter for V_{GS}=0V, V_{GS}=0.5V & V_{GS}=1.0V

I_{DS} versus V_{DS} curves is shown in fig. 7. For DG MOSFET, gate voltage (V_{GS}) is set 0V, 0.5V & 1.0 V while drain voltage (V_{DS}) is ramped from 0 V to 1.0 V by a voltage step of 0.1 V.

Sub threshold voltage, I_{OFF} & I_{ON} Current.

It is important to extract is to determine the threshold voltage, V_T the value of gate voltage when transistor start 'ON' and to investigate the ratio of on-off current, I_{ON}/I_{OFF}. V_T is extracted when I_{DS} is minimum value where the Dirac point as inversion point from hole conductance change to electron conductance. It is also can determine when transconductance, gm (V_{GS}) is equal to zero. Thus, V_T is extracted when V_{DD} equal to 0.1V while gate voltage is ramped from 0 V to 1.0 V by a voltage step of 0.1 V.

Transistor off-state current, I_{OFF} is the drain current when the gate-to-source voltage is zero (V_{GS}=0V). There are many factor can influent I_{OFF} such as V_T, channel physical dimensions, channel / surface doping profiles, drain / source junction depth, gate oxide thickness and V_{DD}. The other current that flows between source and drain when transistor is in the on-state, is called I_{ON} which defined as maximum value of I_{DS}. Since the current is related to V_T, thus this study also implements the formula to find the exact value for I_{ON}, V_{GS}-V_T = 1V as in conventional MOSFET. Thus here takes value of I_{ON} at bias V_{DD}=0.1 V and V_{GS} equal to 1.0V (maximum range).
V_T is 0.107 V for V_{DD} = 0.1 V
I_{OFF} is 0.198 nA for V_{DD} = 0.1 V
I_{ON} is 602 µA for V_{DD} = 0.1 V for DG MOSFET.

III. DESIGN OF SINGLE GATE MOSFET (SG MOSFET)

For designing the proposed device and its simulation, ATLAS device simulator tool of Silvaco TCAD is used.

A. Device Design

The proposed device is Single Gate MOSFET with gate length Lg of 20nm, gate oxide thickness of 1nm, metal gate with work function explicitly set to 4.17 eV, heavily n-doped (ND=1e+20 CM-3) source and drain region, Si is the channel material with channel doped (ND=2.5e+19 CM-3) and SiO2 is the gate dielectric as per the ITRS 2012 road map. Fig. 8 & Fig. 9 shows the designed SG-MOSFET in Silvaco TCAD tool.

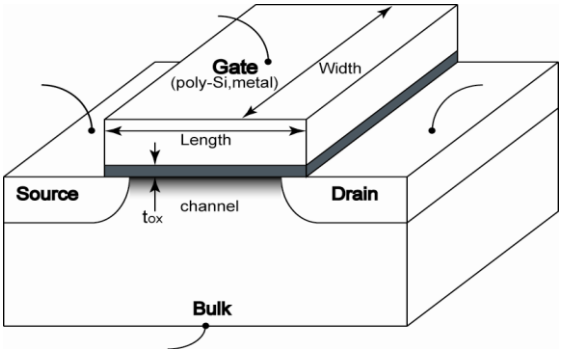


Fig.8 . Schematic structure of SG MOSFET with gate length of 20nm

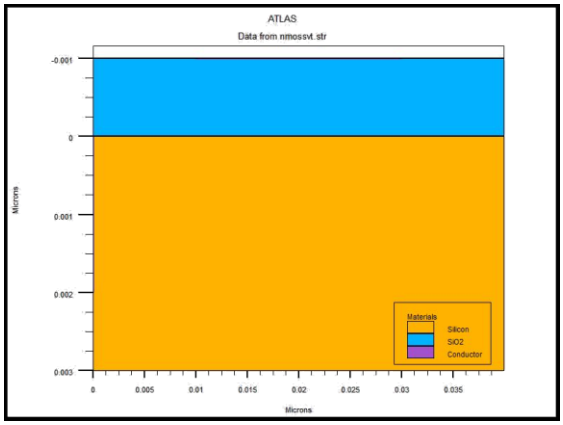


Fig. 9. Two Dimensional Device Structure of SG MOSFET

B. Device Simulation

The modeled device is simulated to obtain the output (I_{DS} versus V_{GS} curve) and (I_{DS} versus V_{DS} curve) for SG MOSFET. Furthermore, some parameters are extracted such as V_T, Sub-threshold, ON current and OFF Current.

I_{DS}- V_{GS} characteristics

The Two models as Shockley-Read-Hall (SRH) model and Lombardi model (CVT) are recommended for physical models for MOS type FETs. For mathematical simulation calculation model, the program select model NEWTON and GUMMEL with maximum trap 4. To generate I_{DS} versus V_{GS} characteristics curve, it is done by obtaining solutions at each step bias points first and then solving over the swept bias variable at each stepped point. V_{DS} value are obtained with V_{GS} = 1.0 V. The outputs from these solutions are saved in .log file (solution file). For each drain bias, .log file is loaded and ramped the gate voltage is performed. The drain voltage (V_{DD}) is set to 0.1 V while gate voltage (V_{GS}) is ramped from0 V to 1.0 V by a voltage step of 0.1V. Finally, one I_{DS}- V_{GS} curves are overlaid using Tony Plot as shown in fig. 10. SG MOSFET. V_{DD}= 0.1 V was chosen to see the current at conduction (inversion layer exists), but at low electric field.

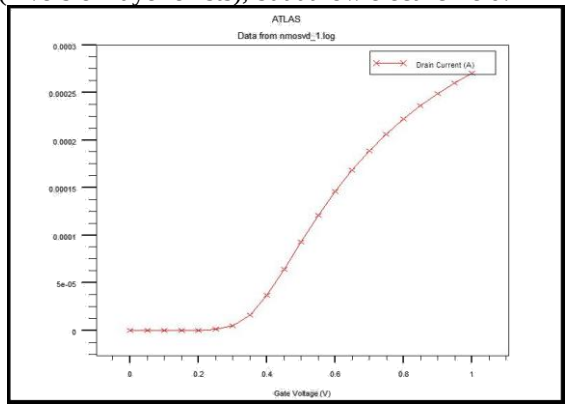


Fig. 10. Transfer characteristics for SG MOSFET with L = 20 nm for V_{DD} =0.1 V, tox= 1 nm

I_{DS}- V_{DS} characteristics

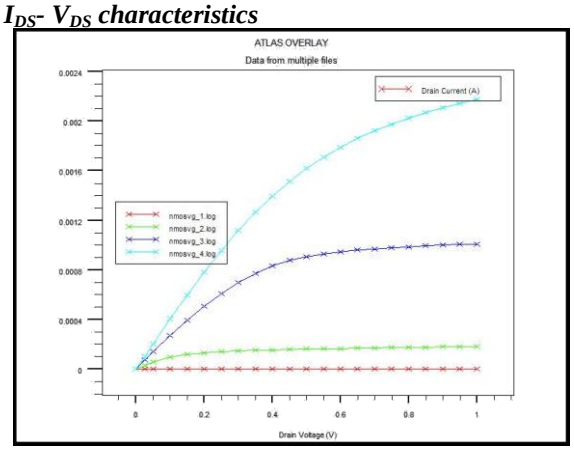


Fig.11. I_{DS} versus V_{DS} of SG MOSFET parameter for V_{GS}=0V, V_{GS}=0.5V & V_{GS}=1.0V

I_{DS} versus V_{DS} curves is shown in fig. 11. For SG MOSFET, gate voltage (V_{GS}) is set 0V, 0.5V & 1.0 V while drain voltage (V_{DS}) is ramped from 0 V to 1.0 V by a voltage step of 0.1 V.

Sub threshold voltage, I_{OFF} & I_{ON} Current.

It is important to extract is to determine the threshold voltage, V_T the value of gate voltage when transistor start 'ON' and to investigate the ratio of on-off current, I_{ON}/I_{OFF}. V_T is extracted when I_{DS} is minimum value where the Dirac point as inversion point from hole conductance change to electron conductance. It is also can determine when transconductance, gm (V_{GS}) is equal to zero. Thus, V_T is extracted when V_{DD} equal to 0.1V while gate voltage is ramped from 0 V to 1.0 V by a voltage step of 0.1 V.

Transistor off-state current, I_{OFF} is the drain current when the gate-to-source voltage is zero (V_{GS}=0V). There are many factor can influent I_{OFF} such as V_T, channel physical dimensions, channel / surface doping profiles, drain / source junction depth, gate oxide thickness and V_{DD}. The other current that flows between source and drain when transistor is in the on-state, is called I_{ON} which defined as maximum value of I_{DS}. Since the current is related to V_T, thus this study also implements the formula to find the exact value for I_{ON}.. Thus here takes value of I_{ON} at bias V_{DD}=0.1 V and V_{GS} equal to 1.0V (maximum range).

V_T is 0.289 V for V_{DD} = 0.1 V
I_{OFF} is 0.198 nA for V_{DD} = 0.1 V
I_{ON} is 270 µA for V_{DD} = 0.1 V for SG MOSFET.

IV. RESULT

Both structure of SG MOSFET and DG MOSFET has designed in silvaco TCAD tool at 20 nm and results has presented. The comparative results are shown in table 1 for V_T, Sub Vt slope, I_{OFF} & I_{ON} for V_{DD}=0.1 V. From table it is clear that DG

MOSFET is having good control over current as I_{ON} is increased from 270 µA to 602 µA. This will leads to reduction in leakage power in the device & hence to the whole circuit. The V_T (Threshold Voltage) is 2.7 times greater than & I_{ON} of DG MOSFET 2.2 times smaller than the conventional Bulk (Single Gate) MOSFET.

TABLE I. EXTRACTED DATA OF DG MOSFET & DG CNFET WITH LG=20NM

For V_{DS} = 0.1 V	V_T (V)	Sub Vt Slope (mv/dec)	I_{OFF} (nA)	I_{ON} (µA)
SG MOSFET	0.289 V	65.5	0.198	270
DG MOSFET	0.107 V	64	158	602

V. CONCLUSION

Short channel effect can be reduced by multigate MOSFETs. Two FET structures have been designed using Silvaco TCAD tool at 20nm technology & comparing the results of Single gate MOSFET & Double Gate MOSFET. Improvement in the device reliability with better reduction of Short Channel Effects has been observed through the simulation results by proper tuning of the channel thickness to ensure the volume inversion. Several structures have been proposed: planar & Non planar. DG MOSFET with planar structure is so far the most promising. Experimental results has presented, the new structure DG MOSFET possesses excellent sub threshold and output characteristics without short-channel effects, demonstrating the shortest gate length. Results shows that leakage current in SG MOSFET is much smaller as compared to that of DG MOSFET, whereas the ON current in DG MOSFET is much larger as compared to that of SG MOSFET. The V_T (Threshold Voltage) is 2.7 times greater than & I_{ON} of DG MOSFET 2.2 times smaller than the conventional Bulk (Single Gate) MOSFET.

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